UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,956	12/20/2001	Benjamim Tang	35706.5700/65	5412

7590 08/23/2005

Michelle R. Whittington, Esq.
SNELL & WILMER, L.L.C.
One Arizona Center
400 East Van Buren
Phoenix, AZ 85004-2202

EXAMINER	
ARTHUR JEANGLAUDE, GERTRUDE	

ART UNIT	PAPER NUMBER
3661	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,956	TANG ET AL.	
	Examiner	Art Unit	
	Gertrude Arthur-Jeanglaude	2144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/27/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Gaudet (U.S Patent No. 6,285,726).

As to claims 1, 10, 17, 23, 29, Gaudet (U.S Patent No. 6,285,726) discloses a PLL/DLL dual loop data serializer comprising: a phase lock loop (PLL) as shown in Fig.3 including, a phase frequency detector (PFD) receiving a local clock, a voltage controlled oscillator (VCO), a loop filter coupled to said PFD and to the VCO, the loop filter configured to suppress VCO phase noise, and a phase shifter coupled to the VCO and configured in a feedback loop with the PFD; a delayed lock loop (DLL) (deayed interpolator as shown in Fig. 5; also see col. 1, lines 6-14) having a digital loop filter (160) as shown in Fig.5 (also see col. 3, lines 18-19) coupled to a phase detector (158) and to the phase shifter of the PLL; a FIFO register receiving a parallel data input and outputting a signal to the phase detector; and a PISO serializer The PHY layer 14 is used as a serializer; see col. 1, lines 29-31) receiving an input from the FIFO and outputting serialized data (See Figs. 3-4; col. 2, lines 34-

67).

As to claim 2, Gaudet discloses the DLL is embedded in the PLL as shown in Fig. 5.

As to claims 3, 26-28, Gaudet discloses the PLL locks to the signal from the FIFO to the phase detector (See col. 3, lines 17-20).

As to claims 4-5, 19-20, 32, Gaudet discloses the loop filter of the PLL comprises a wideband filter (160) and the loop filter of the DLL comprises a narrowband filter (60) as shown in Fig. 2.

As to claim 6, Gaudet discloses the signal to the phase detector comprises a FIFO fill level indicator (See col. 5, lines 54-67; col. 6, lines 35-59).

As to claims 7, 14-15, 25, 33-34, Gaudet discloses the phase detector is configured to translate the FIFO fill level into a digital value (logical operation; see col. 7, lines 5-14) and translating the FIFO fill level to an integrating value.

As to claims 8, 16, 35, Gaudet disclose the serializer for use in a plesiochronous system (See col. 5, lines 26-66).

As to claim 9, Gaudet discloses a dual loop retimer comprising the data serializer as shown in Fig.3.

As to claim 11, Gaudet discloses the step of outputting a synthesized clock (See col. 3, lines 27-41).

As to claims 12-13, Gaudet discloses the PLL filtering step comprises wide bandwidth filtering (160) and the DLL filtering step comprises narrow bandwidth filtering (60) as shown in Fig.2.

As to claim 18, Gaudet discloses the DDLL comprises a phase detector and a digital loop filter (See col. 3, lines 17-20).

As to claim 21, Gaudet discloses the serializer comprises a dual bandwidth (See col. 8, lines 47-67).

As to claim 22, Gaudet discloses the DLL loop filter comprises a narrow bandwidth and the PLL loop filter comprises a wide bandwidth (See col. 7, lines 60-67) also see filters 60, 160.

As to claim 24, Gaudet discloses synthesizing step comprises phase locking the VCO to a local reference (col. 2, lines 34-56).

As to claim 30, Gaudet discloses the step of outputting a synthesized clock (See col. 2, lines 57-65).

As to claim 31, Gaudet discloses the step of phase locking the VCO of the PLL to a local reference to suppress a phase noise of the VCO (See Fig.2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gertrude Arthur-Jeanglaude whose telephone number is (571) 272-6954. The examiner can normally be reached on Monday-Friday from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wiley David can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gertrude A. Jeanglaude
GERTRUDE A. JEANGLAUDE
PRIMARY EXAMINER

GAJ
GAJ
August 17, 2005